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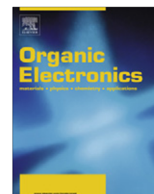

# Capacitance–voltage characteristics of P3HT:PCBM bulk heterojunction solar cells with ohmic contacts and the impact of single walled carbon nanotubes on them

Arun Tej Mallajosyula *, S. Sundar Kumar Iyer, Baquer Mazhari

*Department of Electrical Engineering and Samtel Centre for Display Technologies (SCDT), Indian Institute of Technology Kanpur, Kanpur 208016, India*

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ABSTRACT

Capacitance–voltage (*C*–*V*) characteristics of P3HT:PCBM devices of two different thicknesses are correlated with current density–voltage (*J*–*V*) characteristics. The rising portion of the *C*–*V* characteristics coincides with the exponential current density below the built-in voltage. The negative capacitance (NC) of these devices is a low frequency phenomenon and it occurs in trap-free space charge limited current (SCLC) regime. The onset frequencies of NC for devices with and without SWNTs also do not follow direct relation with effective mobility. The NC in thin devices has non-monotonic change with voltage for thin devices showing that interface state kinetics can be the reason for its occurrence. The NC of thick devices, on the other hand, increases monotonically with voltage showing that bulk properties dominate in these. Addition of SWNTs to these devices for efficiency improvement does not modify their built-in voltage. Also, the SWNTs do not affect the forward NC behaviour. However, the devices containing SWNTs show NC in reverse bias also which has different frequency dependence with voltage. The reverse bias NC is attributed to the large non-linear reverse current by charge injection into the additional energy levels introduced by SWNTs.

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## 1. Introduction

Recently, it has been shown that addition of single walled carbon nanotubes (SWNTs) to polymer solar cells can enhance their efficiency [1–5]. In the particular case of poly-(3-hexylthiophene) (P3HT) based solar cells; SWNTs increase the efficiency by helping in charge transport. Hence, understanding the physics of charge transport in polymer-nanotube solar cells would be necessary to improve their performance. Capacitance (*C*) and admittance spectroscopy are being used to analyse charge transport in organic semiconductor devices [6–9]. Combined with the current density–voltage (*J*–*V*) data, the *C*–*V* characteristics can provide better insights into the physical processes taking place in these devices. Bisquert et al. [10] have used *C*–*V* characterisation under both light and dark conditions to show that the slow exchange kinetics of surface states limit the performance of P3HT: [6,6]-phenyl C61-butyric acid methyl ester (PCBM) bulk heterojunction solar cell. van Mensfoort and Coehoorn [11] have showed that the peak obtained in *C*–*V* characteristics is directly related to the built-in voltage ($V_{bi}$) of the device. This method of $V_{bi}$ determination is more accurate than that using *J*–*V* characteristic in semi-log scale.

Negative capacitance (NC) has been widely studied in semiconductor devices at both low and high frequencies [12–22]. Shulman et al. [12] have given a general treatment to the occurrence of NC. They have shown that NC occurs when a dc bias is superimposed with ac signal on a device which has relaxation phenomena associated nonlinear *J*–*V* characteristics. According to their general mathematical analysis, the combination of nonlinearity and dc bias results in an additional term to the ac current. This

* Corresponding author. Tel.: +91 512 2597924.
*E-mail address:* aruntej@gmail.com (A.T. Mallajosyula).

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current can lag behind voltage giving an inductive effect. Using a different approach, again as a general case, Ershov et al. [13] explained that the NC phenomenon can be understood from the time domain analysis of transient currents where the relaxation component of total capacitance, due to sources such as recombination, traps and impurities, interface effects, and charge generation mechanisms, can result in NC.

Low frequency NC phenomenon is widely observed in organic devices. In organic light emitting diodes, NC was seen to occur in the light emission regime which is indicative of the relation between NC and *e–h* pair recombination under bipolar injection regime [14]. Gommans et al. [15] have shown for metal–insulator–metal structure that NC can be obtained at low frequencies with bimolecular recombination in the drift–diffusion framework. While the physical reason for the occurrence of NC is the delay in the buildup of space charge, the strength of recombination determines the magnitude of NC in this case. Lungenshmeid et al. [16] have reported large negative capacitance in P3HT:PCBM solar cells which gets reduced under illumination and they have attributed this inhibition to photocarriers and re-emission of trapped carries. Bisquert et al. [17] have proposed a kinetic model to describe NC in organic devices which is based on the sequential hopping of electrons from metal to interfacial states to bulk states under non-equilibrium conditions. Such non-equilibrium condition occurs when the rate of electrons populating interfacial states differs from the rate of electrons depopulating bulk states. That is, according to this model, NC phenomenon in organic devices occurs because of injection process itself. It is also possible that a combination of these phenomena can occur in a device. The voltage variation of onset frequency of NC has been related to the carrier mobility by Pingree et al. [18] and Gommans et al. [15].

In this paper, the *C–V* characteristics of P3HT:PCBM devices with Indium Tin Oxide (ITO) and *Ca* as electrodes are shown in both bias directions. For each of these characteristics, the effects of adding SWNTs with metallic characteristics are shown. These characteristics are correlated with *J–V* characteristics to show that NC occurs in the space charge limited current region. Devices with two different thicknesses are used to show that interface kinetics may determine NC in thin devices. Frequency variation of capacitance is also given to show that NC is a low frequency phenomenon and that the onset frequency of NC may not be directly related the charge carrier mobility. That the observed NC is indeed device behaviour has been ensured by measuring the cable and lead inductance values and by testing the impedance measurement equipment accuracy at current levels higher than the device dc currents.

## 2. Experiment details

### 2.1. Device fabrication

The structure of the devices fabricated was ITO|PEDOT:PSS|buffer|P3HT:PCBM:SWNT|*Ca*|*Al*. Spin coating and vacuum thermal evaporation methods were used to deposit organic and metal layers respectively. The buffer layer is of P3HT:PCBM material. The concentration of SWNTs used is 0.75 wt.% of P3HT:PCBM. Detailed fabrication and device performances have been published elsewhere [5,23]. Importantly, the buffer layer method has the advantage of higher open circuit voltage as it avoids direct shorting of SWNTs between anode and cathode. Devices with and without SWNTs are compared here and the thickness values mentioned for the active layer include the buffer layer. Also, SWNTs were not functionalised in order to avoid potential problem of modification of side-wall energetics by the functional group attached. Instead, they were directly dispersed using high power ultrasonication and surfactants were not used because they can result in residue being left over in the active layer. In other words, only pure SWNTs will be inside P3HT:PCBM matrix without any extraneous materials and they directly interact with P3HT:PCBM molecular orbital energy levels. The capacitance measurements were performed using an Agilent 4924A impedance analyser.

### 2.2. Ensuring the accuracy of measurement

It is important to verify the accuracy of the measured capacitance values before attributing any physical phenomena of the devices to them. Consider the complete measurement system which includes the soldered contacts. One can assume a worst case scenario to test the capability of the system. For this case, we check if the system can measure a capacitance which is at least one order lower than the values we obtained for our devices. Specifically, we measured 1 nF capacitance in parallel with different resistor values. The resistor values are chosen so that the current levels will be in mA as were obtained in our actual devices, i.e., the conductance values were chosen to be of similar values as that of our devices. We varied series resistance with values ranging from zero to at least two to three times higher than the ITO contact resistances in our devices. The voltage levels were varied from 0 to 5 V to obtain measurement for different currents. For example, one such plot of measured capacitances at extreme current levels for 0 V and 5 V is shown below in Fig. 1.

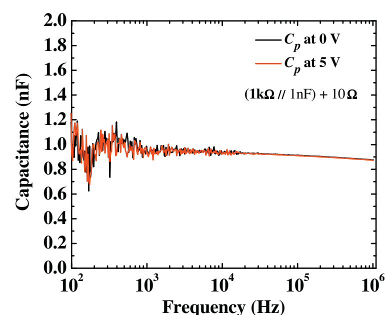


**Fig. 1.** An example of capacitance–frequency plots obtained during equipment capability testing. A capacitance of 1 nF is measured with a 1 kΩ resistor connected parallel to it. A series resistance of 10 Ω is used. Other resistor values lower than these values are also used. The figure shows two plots at two voltages of 0 V and 5 V. The resistor values are chosen so that the currents are in the range of few mA as obtained in actual devices.

As can be seen, the measured value of capacitance continues to be almost same at both current levels with error <20% for low frequencies of 40 Hz–1 kHz and <1% at frequencies >10 kHz. Thus, we ensure that the measurement equipment can measure capacitances of our devices which are much larger than the test capacitor used. For example, at 5 V, our devices showed capacitance of few orders of magnitude higher than 1 nF at low frequencies and about 10–20 times higher than 1 nF at frequencies up to 1 MHz. Hence, we can say that the measured capacitance values can be attributed to device itself.

In capacitance and impedance measurements, it is also important to verify that parasitic inductances are not affecting the measured values. This is more so in the case of devices having large conductance and/or leakage currents. Butcher et al. [24] have shown that typical lead inductances from measurement leads are sufficient enough to cause negative capacitance (NC) to appear. Fig. 2 can be used to understand how the measurement system extracts capacitance and conductance values from a device. The system assumes that the device is a parallel combination of only these two components while there can actually be a series resistance ($R$) and inductance ($L$) associated with the device. Here, the measured capacitance and conductance values are indicated by $C_m$ and $G_m$ respectively while the actual values are indicated by $C$ and $G$.

Translating the total capacitance and conductance values of the actual device to the measured values, we can easily arrive at Eqs. (1) and (2) for $G_m$ and $C_m$, respectively, where $\omega = 2\pi f$, $f$ being the applied frequency of measurement,

$$G_m = \frac{\frac{G}{G^2+(\omega C)^2} + R}{\left(\frac{G}{G^2+(\omega C)^2} + R\right)^2 + \left(\omega L - \frac{\omega C}{G^2+(\omega C)^2}\right)^2} \tag{1}$$

$$C_m = \frac{\frac{C}{G^2+(\omega C)^2} - L}{\left(\frac{G}{G^2+(\omega C)^2} + R\right)^2 + \left(\omega L - \frac{\omega C}{G^2+(\omega C)^2}\right)^2} \tag{2}$$

In these equations, the denominators on the right hand side are in sum of squares form and hence they will be positive. From the numerator of Eq. (2), it can be seen that $C_m$ can become negative only when $L$ is greater than $C/[G^2+(\omega C)^2]$. At low frequencies, this relation would be $L > C/G^2$. It is clear that when $C$ is low or $G$ is high or both, there can be NC due to $L$.

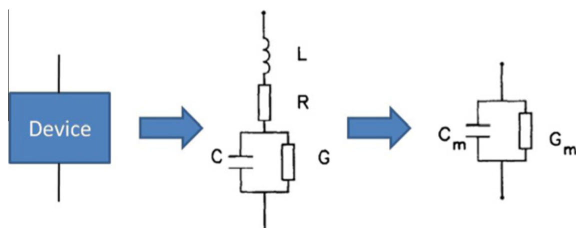


**Fig. 2.** Schematic of a two terminal device showing how the extracted capacitance and conductance values by the measurement system will be different from the actual values in the presence of lead inductance and resistance.

Let us consider the typical values for the cables used for capacitance and impedance measurement. These can be calculated from the cable specifications given by the manufacturer (*Agilent*) as shown in Fig. 3. Here, $Z_o$ and $t_d$ denote the impedance and time delay due to the cable. These quantities are given by Eqs. (3) and (4) using which we can calculate the total capacitance and inductance values ($C_{Total}$ and $L_{Total}$) to be equal to 0.12 nF and 0.30 μH, respectively.

$$Z_o = \sqrt{\frac{L_{Total}}{C_{Total}}}. \tag{3}$$

$$T_d = \sqrt{L_{Total} C_{Total}}. \tag{4}$$

Now, let us look at the typical values obtained for our device (given in later sections) – at 2.5 V, $C$ = 8.5 nF and $G$ = 8.9 mS and at 4.0 V, $C$ = 31.1 nF and $G$ = 17.5 mS. These give $C/G^2$ values of 111 μH and 101 μH, respectively which are more than 300 times the cable inductance. Thus, we can be sure that the cable inductance is not the cause for NC in our devices.

## 3. Results and discussion

### 3.1. C–V characteristics of P3HT:PCBM devices

The $C$–$V$ characteristics of P3HT:PCBM devices at 100 Hz for two different thicknesses of 125 nm and 80 nm are shown in Fig. 4. It is seen that the peak voltage for both devices is the same. This is expected since this peak voltage is directly related to the $V_{bi}$ [11] and both devices have same electrodes. As expected, the zero bias capacitance is lower for thicker device. This is because the capacitance of a parallel plate structure, by definition, is inversely proportional to the thickness. The ratio of zero bias capacitances for 80 nm and 125 nm devices is 1.412 which is close to the expected value of the ratio of thicknesses (1.56). The accuracy of our thickness profilometer is ±5 nm for 0.3 mm range. Hence, the deviation in capacitance is within the expected range. The difference in zero bias capacitances may not be readily apparent in the Fig. 4 because the peak magnitude is large (8 times zero bias value for 125 nm device) which swamps the appearance of this 1.412 times difference. It can be observed that the capacitance peak increased for thicker device. One possible reason might be because of increased amount of injected majority carriers being accumulated in the thicker device than in the thinner device.

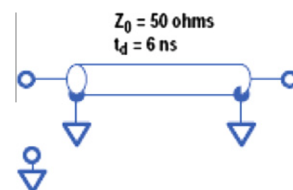


**Fig. 3.** Typical cable impedance and time delay values (source: *Agilent Equipment Manuals*).

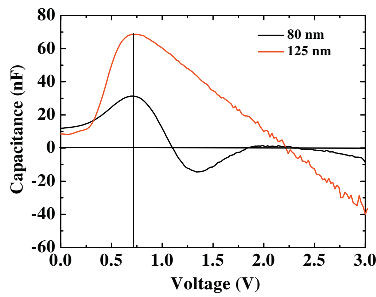


**Fig. 4.** Low frequency *C–V* characteristics of P3HT:PCBM devices with two different thickness values. It can be seen that thicker devices show higher peak capacitance and also larger NC. Both devices have same area of 0.2 $cm^2$ and the measurement frequency was 100 Hz.

Comparing the *C–V* plots with the *J–V* characteristics as shown in Fig. 5, the almost constant capacitance region corresponds to the low current regime and the increasing capacitance region coincides with the rising current regime which has a high slope of 8.04. Usually, such high slopes are indicative of trap filling region if the devices were having zero $V_{bi}$. However, the devices presented here have a $V_{bi}$ of nearly 0.93 V (obtained using the method given by van Mensfoort and Coehoorn [11]). Hence, it can be said that the capacitance increase region corresponds to the exponentially raising current below $V_{bi}$. The peak voltage in *C–V* characteristics is closely related to the onset of recombination as was observed in OLEDs [14].

If we take $V_{bi}$ into account and plot the *J* vs $(V - V_{bi})$ characteristics for voltages above $V_{bi}$, the slope we obtain is 1.9 which is indicative of space charge limited current (where one would expect a slope of 2 in an ideal case). This is shown in Fig. 6. This value of slope indicates that there is no effect of traps in the high voltage range above $V_{bi}$. The corresponding plots of *C–J* vs *V* and *J* vs $(V - V_{bi})$ for 80 nm devices are shown in Figs. 7 and 8, respectively. The capacitance decrease region overlaps with trap-free space charge limited current (TFSCLC) of the device. It can be seen that NC occurs in both 125 nm and 80 nm devices. Interestingly, for the thin P3HT:PCBM device we see that the capacitance increases from NC to zero and then becomes negative again. This non-monotonic behaviour

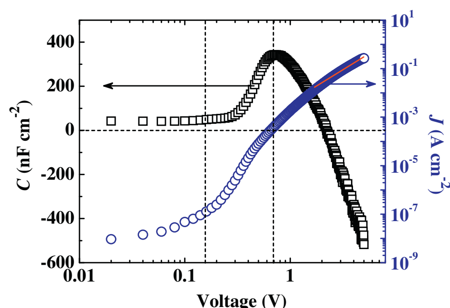


**Fig. 5.** Variation of per unit area capacitance and current density with voltage of a 125 nm P3HT:PCBM device showing that the reduced capacitance occurs in the bulk injection region of device operation, i.e., above $V_{bi}$. The voltage and current density are in logarithmic scale.

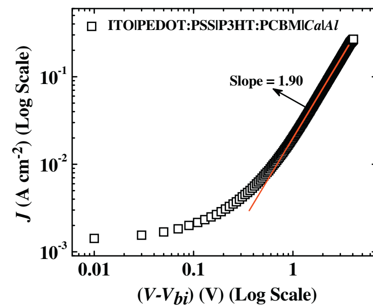


**Fig. 6.** *J–V* characteristics of 125 nm thick P3HT:PCBM device taking built-in voltage into account.

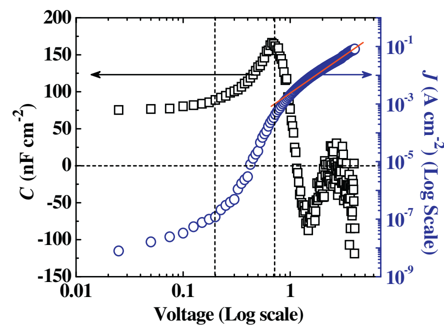


**Fig. 7.** Variation of per unit area capacitance and current density with voltage of a 80 nm P3HT:PCBM device showing that the reduced capacitance occurs in the bulk injection region of device operation i.e., above $V_{bi}$. The voltage and current density are in logarithmic scale.

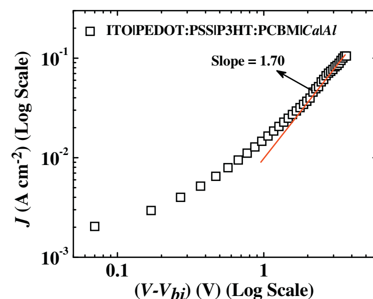


**Fig. 8.** *J–V* characteristics of 80 nm thick P3HT:PCBM device taking built-in voltage into account.

qualitatively follows the model predicted by Bisquert et al. [17]. According to this model, the charge injection process with the device under the condition that the interfacial states are not in equilibrium with injecting electrode is the reason for it. Therefore, NC is determined by the interface kinetics. This model, though derived in the context of polymer light emitting diodes, can be applicable to polymer bulk heterojunction solar cells also since the injection process (through interfacial states) in both device essentially follow the same sequential hopping principle at metal–organic interface. Such non-monotonous NC is not observed for thicker device in the voltage range used for

measurement. In comparison to thicker device, in thinner devices, the effect of interface would be relatively more dominant and the interface will have a larger effect on the device capacitance. Thus, bulk transport and interface kinetics seem to play dominant roles in determining NC behaviour for thick and thin devices respectively.

### 3.2. Effect of SWNTs

The *C–V* characteristics of P3HT:PCBM devices are compared with P3HT:PCBM:SWNT devices in Fig. 9. It can be seen that the capacitance is nearly same for both devices in forward direction. This is because the current densities for voltages above $V_{bi}$ and in space charge region are almost same for devices with and without SWNTs. With SWNTs, the $V_{peak}$ obtained is lower than that of P3HT:PCBM by 0.04 V. Hence, the overall variation in $V_{bi}$ cannot be more than 0.06 V which can be the generally observed device-to-device variation as well. We can say that at low concentrations, SWNTs do not change the $V_{bi}$ of the device.

The *C–V* characteristics in the reverse bias direction, however, are affected by the addition of SWNTs. For example, consider the characteristics of 125 nm devices we have reported in [23], as shown in Fig. 10. While the P3HT:PCBM devices show a positive capacitance corresponding to their geometric capacitance, the P3HT:PCBM:SWNT devices show a negative capacitance. This behaviour can be understood if we consider that with SWNTs, large reverse current flows through the device in reverse bias. Such large current is due to charge injection into the energy levels of SWNTs. These *J–V* characteristics are compared in Fig. 11. This current is only an order of magnitude lower than the forward current. Such high dc current with non-linear characteristics would result in NC as explained by Schulman et al. [12]. The reverse current can result in space charge as well as recombination through SWNT levels. Also, since injection process itself can cause NC, the large injection through SWNTs can also be a cause of NC. In other words, any of the reasons that apply to the forward bias NC can apply to reverse bias NC as well when SWNTs are introduced in the device. This similarity is also supported by the observation that the reverse bias NC is also a low frequency phenomenon like the forward bias NC as seen from Figs. 12 and 13.

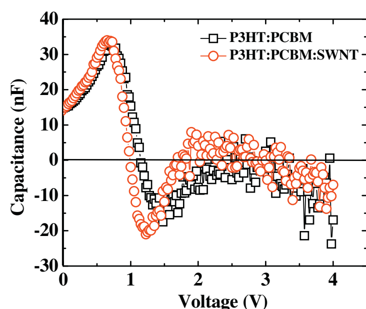


**Fig. 9.** *C–V* characteristics of 80 nm P3HT:PCBM and P3HT:PCBM:SWNT solar cells at low frequencies (100 Hz). The area of the devices is 0.2 cm$^2$.

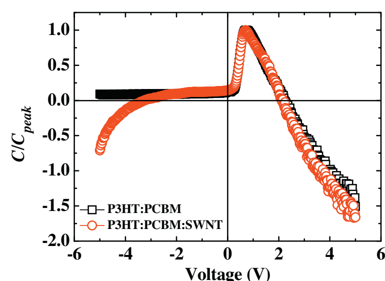


**Fig. 10.** *C–V* characteristics of 125 nm thick solar cells at low frequencies (100 Hz). The area of the devices is 0.2 cm$^2$.

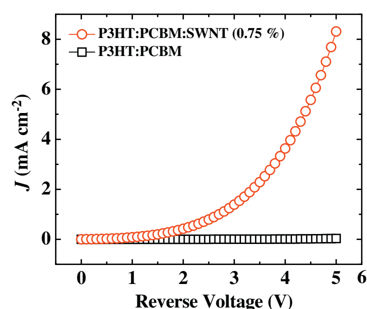


**Fig. 11.** *J–V* characteristics of P3HT:PCBM and P3HT:PCBM:SWNT devices under reverse bias conditions.

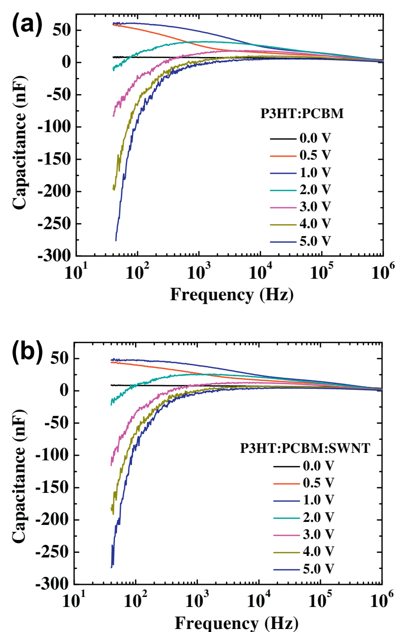


**Fig. 12.** Frequency dependence of capacitance of (a) P3HT:PCBM and (b) P3HT:PCBM:SWNT devices for forward bias showing that the observed NC is a low frequency phenomenon.

### 3.3. Onset frequency of negative capacitance

The onset frequency $f_o$ of NC has been related to the charge carrier mobility $\mu$ in organic semiconductor

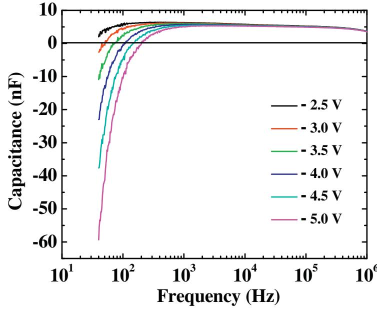


**Fig. 13.** Frequency dependence of capacitance of P3HT:PCBM and P3HT:PCBM:SWNT devices for reverse bias. The reverse bias NC for P3HT:PCBM:SWNT devices is also a low frequency phenomenon like in the forward bias case.

devices. In small molecule based organic light emitting diodes, Pingree et al. [18] have observed that $f_o$ varies linearly with $E^{1/2}$ where $E$ is the applied electric field. From this, correlation has been drawn with $\mu$ which also was known to vary linearly with $E^{1/2}$ since their devices follow Poole–Frenkel theory. However, this cannot be applied in our case because both P3HT:PCBM and P3HT:PCBM:SWNT devices have shown slopes of nearly 2 in the log $J$–$V$ characteristics corrected for $V_{bi}$. This is indicative of trap free SCLC (TFSCLC) following simple $V^2$ power law equation and hence field dependent $\mu$ cannot be used here.

On the other hand, H.H.P. Gommans et al. [15] have shown that $f_o$ varies as $(V/d^2)(\mu_n \cdot \mu_p)^{0.62}$ for polymer light emitting diodes and bulk heterojunction solar cells ($\mu_n$ and $\mu_p$ are the electron and hole mobilities). This has been correlated with the characteristic frequency of TFSCLC being proportional to $\mu V/d^2$. The correlation can be understood from the equation for bipolar TFSCLC [25] as given by:

$$J_{\mathrm{Bipolar}} = \left(\frac{9}{8}\right)\epsilon_o \epsilon_r \mu_{\mathrm{eff}} V^2 d^{-3}. \tag{5}$$

where $\mu_{\mathrm{eff}} = \left(\frac{2}{3}\right)\left[2\pi \cdot (\mu_n \cdot \mu_p)(\mu_n + \mu_p/)\mu_o\right]^{1/2}; \mu_o = \frac{\epsilon_o \epsilon_r VS}{2q}$

In these equations, $\mu_{\mathrm{eff}}$ is the effective mobility, $\mu_o$ is the recombination velocity, $v$ is the thermal velocity, and $s$ is the recombination cross-section. The rest of the symbols have the same meaning as was being used throughout the thesis. Assuming that for Langevin recombination $\mu_o$ is proportional to $(\mu_n + \mu_p)$, $\mu_{\mathrm{eff}}$ will be proportional to $(\mu_n \cdot \mu_p)^{1/2}$. Therefore, the $f_o$ should be varying as $(\mu_n \cdot \mu_p)^{1/2} V/d^2$. From detailed numerical simulations, they found that the power of $(\mu_n \cdot \mu_p)$ is 0.62 instead of 0.5. From this method we can see that, for a given mobility, $f_o$ should have a linear relation with $V/d^2$ (=$E/d$). The plots for variation of $f_o$ with $E/d$ (corrected for $V_{bi}$) in log scale are shown in Fig. 14.

It can be seen that the slope is not equal to unity. Instead, the slopes for both P3HT:PCBM and P3HT:PCBM:SWNT devices equal 2.5 in forward bias. Therefore, we can say that this simple direct correlation with TFSCLC is not valid in these devices. This may be because the cause for the occurrence of NC may not be only the lag due to space charge but there can be other contributing factors also. As mentioned earlier, these can be the strength of recombination and the interfacial states. In reverse bias also, the slope for P3HT:PCBM:SWNT device is not unity. In this case, the current is not TFSCLC and as such the slope need not be equal to unity as per the above correlation. However, the reason for higher value of slope (3.4) than in forward bias case is not clear. Unlike the forward bias case, since SWNTs are the major reason for charge conduction and recombination in reverse bias, the difference in slope values may be because of different recombination strengths.

The inductive effect due to current lag in a device is usually represented by a series resistance–inductor ($RL$) circuit element which can also be replaced by its equivalent parallel resistance–capacitance circuit element ($RC$). In such a case, the value of $C$ will be equal to $-G\tau/(1+\omega^2\tau^2)$ where $\tau = L/R$ is the time constant of $RL$ circuit. Thus, the negative capacitance can be expected to vary with frequency as $1/\omega^2$ i.e., NC can be fit to a second order equation in $1/\omega$. In such a case, the total device capacitance can be written as:

$$C = C_{\mathrm{Geom}} + \frac{\alpha}{1+\beta\omega^2}. \tag{6}$$

where $\alpha = -G\tau$ and $\beta = \tau^2$.

For our devices both with and without SWNTs, Eq. (6) gave a moderately accurate fit with adjusted coefficients of determination better than 0.97 in forward bias. This fitting gave nearly same effective time constant values for devices both with and without SWNTs in the range of 2.5–2.9 ms. On the other hand, the reverse bias NC of SWNT devices fit well with adjusted coefficient of determination of 0.99 giving an effective time constants in the range of 5.0–10.0 ms. These $\tau$ values show that the reverse bias NC caused by SWNTs is a slower process compared to forward bias NC.

For specific cases, it may be possible that more than one process simultaneously affect the device capacitance requiring more than a simple $RL$ element for equivalent circuit representation. Such circuit representations have been reported in literature for organic semiconducting devices [18,26,27]. Thus, as a general case, the total capacitance of a device can be written as the sum of its geometrical capacitance $C_{\mathrm{Geom}}$ and other frequency varying terms as:

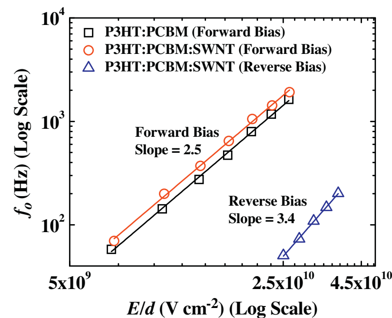


**Fig. 14.** Variation of the onset frequency of negative capacitance $f_o$ with the applied field, $E$. Here, $E$ is taken as $(V - V_{bi})/d$.

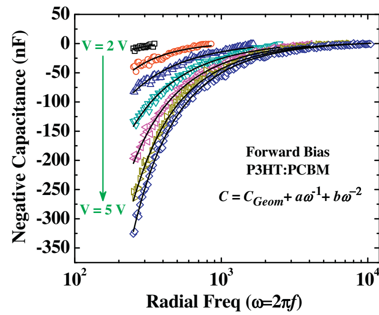


**Fig. 15.** Negative capacitance of P3HT:PCBM devices at various voltages fit to 2nd order equation with inverse of radial frequency as the variable. The value of $C_{Geom}$ is 5 nF.

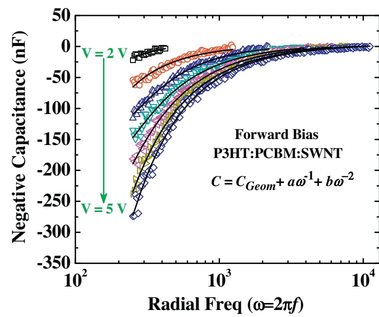


**Fig. 16.** Negative capacitance of P3HT:PCBM:SWNT devices at various voltages fit to 2nd order equation with inverse of radial frequency as the variable. The value of $C_{Geom}$ is 5 nF.

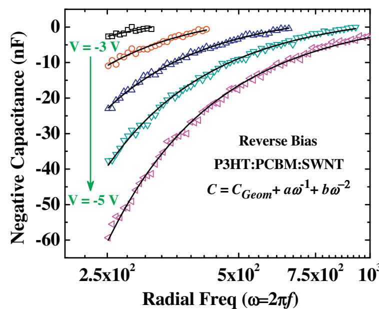


**Fig. 17.** Negative capacitance of P3HT:PCBM:SWNT devices in reverse bias at various voltages fit to 2nd order equation with inverse of radial frequency as the variable. The value of $C_{Geom}$ is 5 nF.

$$C = C_{Geom} + a\omega^{-1} + b\omega^{-2} + c\omega^{-3} \cdots \quad (7)$$

where *a*, *b*, *c*... are the coefficients of 1st, 2nd, 3rd... order processes determining NC. Fitting Eq. (7) with the NC characteristics of our devices, we see that only two coefficients (*a*, *b*) are sufficient for both forward and reverse bias NC. These fits are more accurate in both bias directions with adjusted coefficients of determination better than 0.99. The NC characteristics fitted with Eq. (7) are shown in Figs. 15–17.

Variation of the magnitudes of these coefficients can be used to understand if the same processes are determining

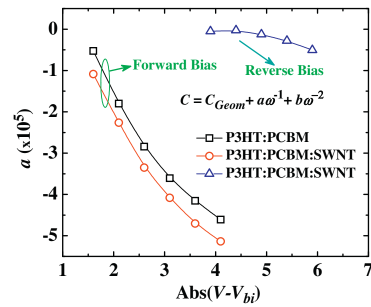


**Fig. 18.** Variation of the coefficient *a* corresponding to any 1st order process affecting negative capacitance of P3HT:PCBM device in forward bias and P3HT:PCBM:SWNT device in both bias directions.

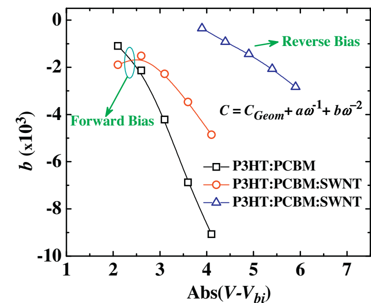


**Fig. 19.** Variation of the coefficient *b* corresponding to any 2nd order process affecting negative capacitance of P3HT:PCBM device in forward bias and P3HT:PCBM:SWNT device in both bias directions.

NC in different devices or for the same device operating under different conditions. These are shown in Figs. 18 and 19. From these figures, it can be observed that coefficient *a* shows nearly same values and voltage dependence for both P3HT:PCBM and P3HT:PCBM:SWNT devices in forward bias. This shows that any 1st order process contributing to NC is same in these devices. The coefficient *b* in forward bias shows different variations with and without SWNTs indicating that probably SWNTs affect a second order process. Both the coefficients in reverse bias for P3HT:PCBM:SWNTs, however, have lower magnitude and slower voltage variation. This shows that the origin of NC in reverse bias due to SWNTs may be different than that in forward bias. More investigations are necessary to understand the exact physical mechanisms for such behaviour.

## 4. Conclusions

For P3HT:PCBM solar cells, two factors – recombination and space charge – result in reducing low-frequency capacitance. This conclusion is obtained when we correlate their *C–V* and *J–V* characteristics. These devices show thickness dependent negative capacitance in forward bias. As opposed to thick devices, thin devices show non-monotonous negative capacitance characteristics. This behaviour is attributed to the domination of charge injection process at the interface over bulk processes in thin devices. While previous works have reported that onset frequency of negative capacitance has direct relationship with charge

carrier mobility, our results show that this simplistic view may not be valid for all cases.

When SWNTs are added to these solar cells for efficiency improvement, they do not have any impact on the peak position of the forward bias *C–V* characteristics. This shows that the SWNTs, though metallic in nature, do not change the effective built-in voltage. SWNTs, however, have a significant impact on the negative capacitance characteristics of P3HT:PCBM solar cells. Specifically, SWNTs result in a negative capacitance in reverse bias. Large conductance with non-linearity is a reason for this behaviour. Frequency variation of negative capacitance with voltage indicates that NC in these devices has contributions from two processes and SWNTs affect the 2nd order process in forward bias. Also, the origin of NC in reverse bias may be different from that in forward bias in P3HT:PCBM:SWNT devices. Further studies are necessary to pin-point the exact physical phenomena resulting in such behaviour.

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